

## **Remarks**

In the Office Action, the Examiner noted that claims 1-79 are pending in the application, and that claims 1-79 are rejected. By this amendment, claims 80-82 have been added. Thus, claims 1-82 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

## ***In the Specification***

In the specification, paragraphs were amended to include the serial number of a co-pending application and the number of a U.S. Patent Application that were incorporated by reference.

## ***In the Claims***

### **Rejection Under 35 USC 102(b)**

The Examiner rejected claims 1-28 and 30-79 under 35 U.S.C. § 102(b), as being anticipated by *Beukema, et al.*, U.S. 2002/0073257 (hereinafter *Beukema*). Applicant respectfully traverses the rejection of claims 1-28 and 30-79.

Generally, *Beukema* teaches a network computing system having end nodes, switches, routers, and links interconnecting the end nodes, switches, and routers. In particular, *Beukema* teaches an InfiniBand network including distinct InfiniBand channel adapters and InfiniBand switches as taught in Applicant's Background section, particularly from page 4, line 7 to page 5, line 13. *Beukema* further teaches employing manufacturer-definable operation codes to define InfiniBand packet types that have the characteristics of reliable packet types to bypass using the queuing structure (queue pairs) prescribed for InfiniBand-defined operation code packet types in order to perform PCI operations over his Infiniband network. *Beukema* teaches a host channel adapter that recognizes a load or store address generated by a host end node processor that is in a range corresponding to a PCI I/O adapter connected to a target channel adapter across the network. In the case of a store, the host channel adapter transmits an InfiniBand packet containing the store data and address across the network to the target channel adapter, which performs a PCI write to the PCI I/O adapter using the store address and data. In the case of a load, the host

channel adapter transmits an InfiniBand packet containing the load address across the network to the target channel adapter, which performs a PCI read of the load address from the PCI I/O adapter to obtain the load data, which it then transmits in an Infiniband packet back to the host channel adapter for provision of the load data to the processor that generated the load. Additionally, *Beukema* teaches the target channel adapter recognizes when the PCI I/O adapter performs a PCI read or write. In the case of a PCI write, the target channel adapter transmits an InfiniBand packet containing the write data and address across the network to the appropriate host channel adapter, which writes the data into the host end node system memory at the specified address. In the case of a PCI read, the target channel adapter transmits an InfiniBand packet containing the read address across the network to the appropriate host channel adapter, which reads the data from the host end node system memory at the specified address and transmits an InfiniBand packet including the data across the network back to the target channel adapter, which performs a PCI write to the PCI I/O adapter with the specified data and address.

#### ***Claims 1-22***

With respect to claim 1, the Examiner asserted that *Beukema* teaches an integrated circuit functioning as an InfiniBand channel adapter and an InfiniBand switch. The portions of *Beukema* cited by the Examiner refer to the network as described above, not to an integrated circuit. Applicant can find no teaching in *Beukema* of an integrated circuit functioning as an InfiniBand channel adapter and an InfiniBand switch and therefore respectfully asserts that *Beukema* does not anticipate claim 1.

Applicant respectfully asserts *Beukema* does not anticipate dependent claims 2-22 because they depend from independent claim 1, which is not anticipated by *Beukema* for the reasons discussed above.

#### ***Claims 23-28 and 30-35***

With respect to claim 23, the Examiner asserted that *Beukema* teaches a transaction switch with a memory that selectively transfers data through the memory between two packetized data devices and between a packetized data device and an addressed data device. Applicant respectfully asserts that *Beukema* does not teach a transaction switch with a memory that selectively transfers data through the memory between two

packetized data devices and between a packetized data device and an addressed data device. As discussed above, *Beukema* teaches an InfiniBand network including distinct InfiniBand channel adapters and InfiniBand switches. InfiniBand channel adapters transfer data between an InfiniBand device and an addressed data device, such as a PCI device, as described in Applicant's Background section, as discussed above; however, *Beukema* does not teach his InfiniBand channel adapters also transferring data between two InfiniBand devices, as recited by claim 23. Similarly, InfiniBand switches transfer data between two InfiniBand devices, as described in Applicant's Background section, as discussed above; however, *Beukema* does not teach his InfiniBand switches also transferring data between an InfiniBand device and an addressed data device, as recited by claim 23. Applicant respectfully asserts that *Beukema* does not teach a transaction switch with a memory that selectively transfers data through the memory between two packetized data devices and between a packetized data device and an addressed data device and therefore does not anticipate claim 23.

Applicant respectfully asserts *Beukema* does not anticipate dependent claims 24-35 because they depend from independent claim 23, which is not anticipated by *Beukema* for the reasons discussed above.

#### ***Claims 36-40***

With respect to claim 36, the Examiner asserted that *Beukema* teaches a plurality of transaction queues associated with each of a plurality of data interfaces configured to store transactions and control logic configured to switch the transactions between the plurality of data interfaces. Applicant can find no teaching in *Beukema* of a plurality of transaction queues associated with each of a plurality of data interfaces configured to store transactions and control logic configured to switch the transactions between the plurality of data interfaces. The Examiner cites the InfiniBand host channel adapter of Fig. 3. of *Beukema* generally, apparently indicating that the Queue Pairs (QPs) of Fig. 3 correspond to the claimed transaction queues and that the InfiniBand ports of Fig. 3 correspond to the plurality of data interfaces. *Beukema* teaches the QPs are a means used by consumers to transfer messages to the host channel adapter InfiniBand ports. Each QP consists of a send work queue and a receive work queue. The consumers are software

that calls an operating system-specific programming interface to place a work request onto a work queue of a QP. (*Beukema* specifically teaches that his method of sending PCI protocol requests across a SAN does not use the QPs, but instead bypasses them; see paragraph 42). However, assuming *arguendo* that the work requests correspond to the claimed transactions, Applicant can find no teaching in *Beukema* of the host channel adapter switching the work requests between the InfiniBand ports. Furthermore, Applicant can find no teaching in *Beukema* of the InfiniBand switches employing QPs, which is not surprising since InfiniBand specifies QPs for channel adapters but does not specify QPs for switches; rather, InfiniBand switches do not receive work requests from consumers, but simply pass packets along based on the destination address in the packet's local routing header. Still further, *Beukema* does not teach disparate data transfer protocols supported by the data interfaces of his switches as recited by claim 36; rather, all the ports of *Beukema*'s switches support the same protocol, namely InfiniBand. For these reasons, Applicant respectfully asserts that *Beukema* does not teach a plurality of transaction queues associated with each of a plurality of data interfaces configured to store transactions and control logic configured to switch the transactions between the plurality of data interfaces and therefore does not anticipate claim 36.

Applicant respectfully asserts *Beukema* does not anticipate dependent claims 37-40 because they depend from independent claim 36, which is not anticipated by *Beukema* for the reasons discussed above.

#### ***Claims 41-62***

With respect to claim 41, the Examiner asserted that *Beukema* teaches an integrated circuit having at least three data interfaces, at least one of them being of a different type than the others. Applicant can find no teaching in *Beukema* of an integrated circuit having at least three data interfaces where at least one of them is of a different type than the others. The Examiner cites the InfiniBand host channel adapter of Fig. 3 of *Beukema*, but does not specifically identify the three data interfaces as claimed. Applicant assumes the Examiner is referring to the InfiniBand ports 312-316 of the host channel adapter. Applicant respectfully points out that the InfiniBand ports 312-316 are all of the same type, i.e., all are InfiniBand ports. The Examiner also refers to paragraph 7, which

teaches processing a PCI transaction across a system area network by employing a host channel adapter and a target channel adapter, which includes a PCI interface. However, Applicant respectfully points out that *Beukema* nowhere teaches an integrated circuit that comprises the host channel adapter and a target channel adapter; rather, the host channel adapter and a target channel adapter are part of a network of distinct channel adapters and switches as taught in Applicant's Background section, as discussed above with respect to claim 1.

Further with respect to claim 41, the Examiner asserted that *Beukema* teaches an integrated circuit having a memory shared by at least three data interfaces for buffering data between the at least three data interfaces and a transaction switch that dynamically allocates portions of the memory to the interfaces for storing data. Applicant can find no teaching in *Beukema* of an integrated circuit having a memory shared by at least three data interfaces for buffering data between the at least three data interfaces and a transaction switch that dynamically allocates portions of the memory to the interfaces for storing data. The Examiner cites the InfiniBand channel adapter of Fig. 3 of *Beukema*; however, because the Examiner does not specifically identify the shared memory element of claim 41, it is unclear to Applicant which element of the channel adapter the Examiner asserts corresponds to the claimed shared memory. Applicant assumes for the sake of efficient prosecution of the instant application the Examiner is indicating either the memory 340 or the virtual lanes 334 correspond to the shared memory of claim 41.

With respect to the virtual lanes 334, although *Beukema* teaches that they buffer data to the channel adapter ports, Applicant respectfully points out that *Beukema* does not teach the virtual lanes are dynamically allocated to the ports, as recited in claim 41; in contrast, the Figure appears to indicate the virtual lanes are associated with a specific port in a fixed fashion.

With respect to the memory 340, *Beukema* teaches that a direct memory access (DMA) entity performs direct memory access operations using the memory 340. Fig. 3 indicates that the memory 340 is not part of the channel adapter itself, but rather is part of the InfiniBand end node containing the channel adapter. However, Applicant notes that Fig. 3 is essentially identical to Figure 14 of section 3.4.2 of the InfiniBand Architecture

Release 1.0 Volume 1 Specification. As the section of the Specification indicates, InfiniBand end nodes generate and consume packets (which *Beukema*'s Background section also teaches) in contrast to InfiniBand switches. As discussed above, *Beukema* does not teach a combined InfiniBand channel adapter and switch; thus, the end node memory 340 would be where InfiniBand packets are generated or consumed, not buffered between the InfiniBand ports of the channel adapter, as recited in claim 41. Finally, *Beukema* does not teach the end node being an integrated circuit.

Thus, Applicant respectfully asserts that *Beukema* does not teach an integrated circuit having at least three data interfaces, at least one of them being of a different type than the others, nor an integrated circuit having a memory shared by at least three data interfaces for buffering data between the at least three data interfaces and a transaction switch that dynamically allocates portions of the memory to the interfaces for storing data, and therefore does not anticipate claim 41.

Applicant respectfully asserts *Beukema* does not anticipate dependent claims 42-62 because they depend from independent claim 41, which is not anticipated by *Beukema* for the reasons discussed above.

#### ***Claims 63-79***

Applicant respectfully asserts that *Beukema* does not anticipate claims 63, 67, and 71 for similar reasons as those discussed above with respect to claim 1. Applicant respectfully asserts *Beukema* does not anticipate dependent claims 64-66, 68-70, and 72-78 because they depend from independent claims 63, 67, and 71, respectively, which are not anticipated by *Beukema* for the reasons discussed above.

With respect to claim 79, Applicant respectfully asserts that *Beukema* does not anticipate claim 79 for similar reasons as those discussed above with respect to claims 1, 23 and 36. Furthermore, the Examiner asserted that *Beukema* teaches a mapping table for storing packet destination identification information and control logic that selectively switches data between a plurality of data devices based on the mapping table information and in response to transactions. Applicant respectfully asserts that *Beukema* does not teach a mapping table for storing packet destination identification information and control logic that selectively switches data between a plurality of data devices based on the mapping

table information and in response to transactions. The Examiner refers to paragraph 77 of *Beukema*. However, Applicant respectfully points out that paragraph 77 teaches that the host channel adapter determines which target channel adapter is to be the destination of a packet based on a store address generated by a CPU, not based on packet destination identification information, as recited by claim 79. That is, the portions of *Beukema* cited by the Examiner teach the host channel adapter creating packet destination information based on a CPU store address, not switching data based on packet destination information stored in a mapping table.

### **Rejection Under 35 USC 103**

The Examiner rejected claim 29 under 35 U.S.C. § 103, as being unpatentable over *Beukema* in view of "Official Notice". Applicant respectfully traverses the rejection of claim 29.

Applicant respectfully asserts *Beukema* does not anticipate dependent claim 29 because it depends from independent claim 23, which is not anticipated by *Beukema* for the reasons discussed above.

The Examiner has indicated additional prior art which is made of record and not relied upon. None of these references anticipate or obviate applicant's invention.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Applicant earnestly requests the examiner to telephone him at the direct dial number printed below if the examiner has any questions or suggestions concerning the application.

Respectfully submitted,

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By: *William J. Hojan*